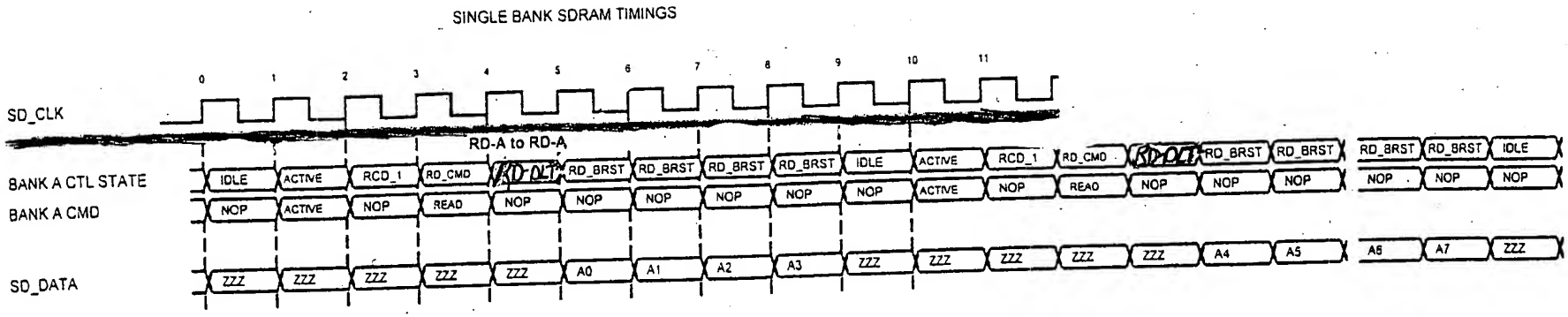

FIG. 15A

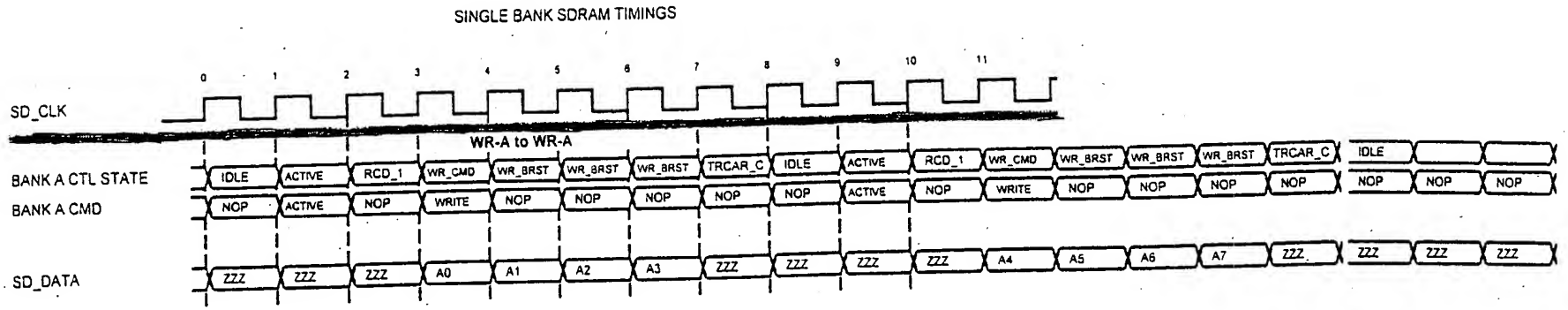

FIG. 15D

TWO BANK SDRAM TIMINGS

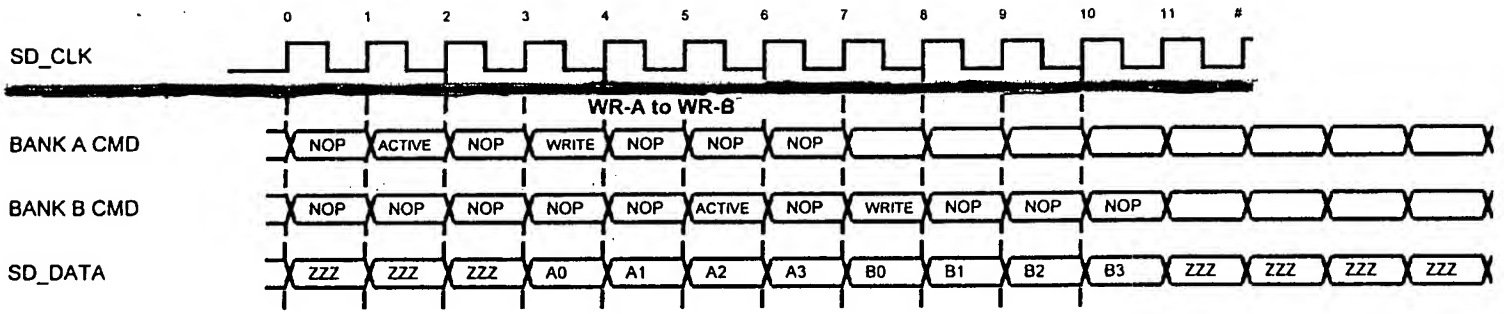

FIG. 16D